multiLane

# ML4004-JIT

## Time Domain Analyzer with Jitter generation


**BERT 3.2 – 5, 6.5 – 15 and 19 – 30 Gbps**
**+ DSO 32 GHz**
**Jitter Generation & Analysis**

**Jitter Injection and Analysis**
**Eye Measurements**
**Eye Mask Test**
**Advanced Pattern Acquisition**
**Pre-emphasis Measurement**
**J2/J9 measurements**
**Scope with integrated CDR**

March 2019

# ML4004-JIT

## Dual-Channel BERT
## And Differential Sampling Scope

## Summary

The **ML4004-JIT** is a state of the art BERT and Digital Sampling Oscilloscope in one compact box.

The BERT features two differential channels, one for AM and PM jitter injection and the other for classical BERT applications.

The DSO performs accurate eye-diagram analysis to characterize the quality of transmitters.

The instrument is optimized for high speed data analysis and is controlled through Ethernet.

The **ML4004-JIT DSO** implements a statistical under sampling technique and features comprehensive software libraries and APIs. It performs various eye and pattern measurements, mask margin tests and jitter analysis on NRZ or PAM-4 data.

## Target Applications

- Compliance testing e.g. OIF-CEI 03.1 and IEEE 802.3bm – the ML4004-JIT features an automated JTOL function.
- Interconnect testing, SFP, SFP28, CFP, CFP2, CFP4, QSFP, QSFP28, …
- Backplane testing
- Interference and Crosstalk testing
- Receiver sensitivity testing

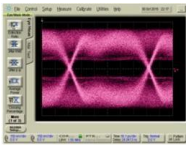
## Key Features

### *PPG and ED*

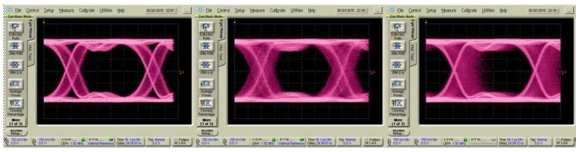
- Data Rates: 3.2-5, 6.5-15 and 19-30 Gbps
- Low power consumption
- Optional BW of 32 or 50GHz
- Automated J2/J9 measurements
- High input BW achieved with industry leading sample-and-hold amplifiers
- Eye Contour measurements above 9 Gbps
- API library with intuitive and simple GUI
- Instant and Real time BER (Bit Error Rate)
- Vertical and horizontal bathtub measurement above 9 Gbps
- PRBS 7, 9, 15, 23, 31 and user-defined pattern generation (up to 40 bits)
- Windows and Linux APIs are provided allowing users to develop their own automated tests

### *Jitter Generation*

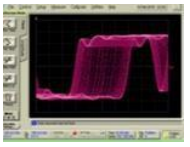
- Typically needed for stressed receiver tests.
- Vertical and Horizontal eye closure
- Amplitude random jitter injection (RJ AM)

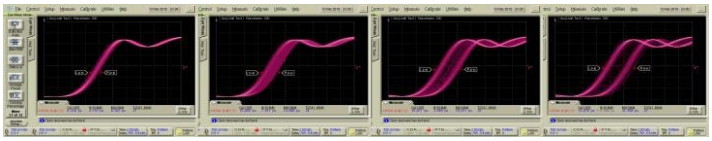


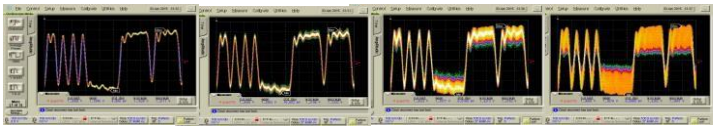
- Sinusoidal and random jitter injection(SJ, RJ PM)



- Phase shifting







## *Digital Sampling Oscilloscope*

- 1200 mVppd input amplitude
- Equipped with a CDR (Clock Data Recovery) circuit, sampling a signal without input clock.

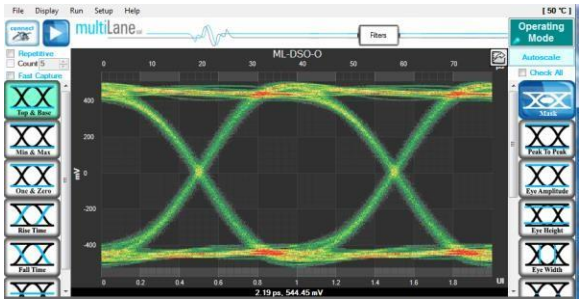



**Figure 1 Eye Diagram Mode**

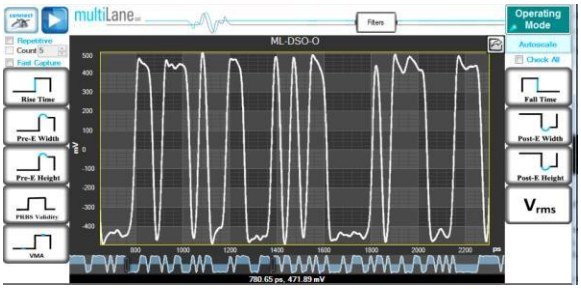



**Figure 2 Pattern Lock Mode**

- Eye opening, height and width, eye amplitude, top, base, Hi, Lo, max, min, etc…

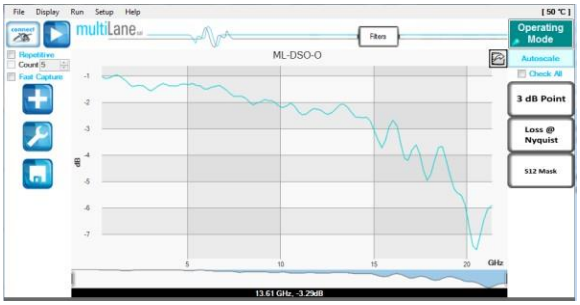



**Figure 3 FFT Mode Displays Frequency Domain Measurements & Enables Importing & Exporting Touchstone Files**

- Total jitter measurement and jitter decomposition
- Rise/ Fall Time, Crossing percentage.
- Zooming, markers, X and Y histogram overlays, statistics over multiple measurements.
- Eye & pattern measurements on specific properties of the pattern.
- Pre and Post -emphasis positive and negative (amplitude and width) measurements.
- DSP filters suite includes Bessel-Thomson, CTLE, FFE, DFE, De-embedding, Moving Averages and Normalizing filters.
- The DSO can be set to continuously capture and save data in an external csv file for later processing.
- Repeatable traceable measurements.
- Capability to save statistical measurements & data files for multiple DSOs simultaneously.

| Electrical Specifications | | |
|---|---|---|
| | Power rating | 12 VDC, 1.2A |
| | Operating temperature range | 0 – 65 °C |
| **PPG1** | Bit Rates | 3.2-5 and 6.5-15 and 19.0-30 Gbps |
| | TX Amplitude Differential | 125-800mV |
| | Patterns | PRBS 7/9/15/23/31 User Pattern 40 bits |
| | TX Amplitude Adjustment | 100 mV on the clean output |
| | Pre-Emphasis | 6db |
| | Pre-Emphasis Resolution | 10 steps |
| | Equalizing Filter Spacing | 1UI |
| | Random Jitter RMS | 250 fs |
| | Rise/ Fall Time (20–80%) | 17 ps |
| | Output Return Loss up to 10GHz | -10.7 dB |
| **ED1** | Error Detector Phase Margin | 5 ps |
| | Error Detector Maximum Input | 1200mV Diff |
| | Phase Scan Resolution | 7 Bits |
| | Vertical Scan Resolution | 8 Bits |
| | Input CTLE Dynamic Range | 10dB |
| | TX/RX and clock connectors | 2.92 mm Connectors |
| | Reference clock Output | Rate / 64, LVPECL ~ 1300 mV |
| **PPG2 JIT** | Bit Rates | 3.2-5 and 6.5-15 and 19.0-30 Gbps |
| | TX Amplitude Differential | 0-2000 mV |
| | Patterns | PRBS7/9/15/23/31 User Pattern 40 bits |
| | TX Amplitude Adjustment | 2 mV |
| | Sinusoidal Phase Modulation | >90 ps |
| | Sinusoidal Jitter Frequency | 0.1 to 80 MHz |
| | Random Jitter RMS | 360 fs |
| | Rise/ Fall Time (20–80%) | 16 ps |
| | TX Skew control | >90 ps |
| | Output Return Loss up to 10GHz | -14 dB |
| | ESD Rating | >6 Gbps io 1000V HBM, 250V CDM<br><6 Gbps io 2000V HBM and 500V CDM |
| | Power Adapter specifications | 12V/1.2A 2.1 x 5.5 mm Centre Positive |
| **DSO** | Input Bandwidth | 32 GHz (50 GHz optional) |
| | Input Amplitude (Single ended) | AC: 600 mVpp S-E |
| | Input Rise / Fall Time | 15 ps |
| | Diff. Input Return Loss | < 12dB |
| | Vertical Resolution | 14 bits |
| | Clock Input Range (Normal Mode) | 50 - 550 MHz |
| | Clock Input Amplitude | 200 - 1000 mV |
| | Input Impedance | 50 Ω |
| | Intrinsic Jitter (excluding DDJ) | 250 fs |
| | Amplitude Error | 10 mV |

| | | |
|---|---|---|
| **DSO** | Data Format Support | NRZ and PAM4 |
| | PRBS Pattern Capture | up to PRBS-13 |
| | Spurious-Free Dynamic Range | 46 dBc at 10 GHz 500mVppd input |
| | Temperature range | 0-65C |
| | Memory Depth | 256K sample |

| Mechanical Specifications | | |
|---|---|---|
| | Dimensions | WxHxL = 21.8 x 8.89 x 30 cm3 |
| | Weight | ~1.5 Kg |

## Technical Drawings